First Determination of Thermal Resistance and Thermal Capacitance of Atomic-Layer-Deposited In_2O_3 Transistors

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Abstract — Electrical and thermal co-design and co-optimization become more and more important for the state-of-the-art monolithic 3D integration. In this work, for the first time, we determined the thermal resistance (R_{TH}) and the thermal capacitance (C_{TH}) of back-end-of-line (BEOL) compatible atomic-layer-deposited (ALD) ultrathin In_2O_3 field-effect transistors (FETs) by measuring the steady-state and transient temperatures of active devices using a thermo-reflectance (TR) imaging system. Through the extracted R_{TH} and C_{TH}, the heat dissipation capability of In_2O_3 FETs is found to be related to the geometry of the transistors. An 83% reduction of R_{TH} and a 379% increase of C_{TH} can be obtained by scaling down the channel length (L_{ch}) of In_2O_3 FETs from 6 μm to 600 nm. This work offers a new methodology to quantitatively study the thermal properties of thin film transistors along with their electrical performance.

I. Introduction

Development of BEOL-compatible devices is significantly important for monolithic 3D integration as a promising solution to increase on-chip transistor density and keep the semiconductor technology moving forward [1–2]. Recently, ALD In_2O_3 FETs have stood out due to their low thermal budget under 350 °C [3], good conformality and uniformity on 3D structure [4], high electron mobility over 100 $cm^2/V\cdot s$ [4], maximum on-current near 20 mA/μm [5] and ultrahigh reliability [6]. One remaining challenge of In_2O_3 transistors is their self-heating effect (SHE), making the devices unstable at high V_{DS} biases thus limiting their achievable high I_{DS} [7–10]. To resolve this issue, a complete quantitative investigation of the thermal properties of In_2O_3 FETs is a must.

In this work, thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) which can quantify the thermal properties of a transistor, are determined for the first time by measuring steady and transient temperatures using a thermo-reflectance (TR) imaging system [11]. From different device geometry, we found that using a high thermal conductivity substrate and scaling down the size of the devices are two crucial ways for better heat dissipation and reduction of the SHE.

II. Experiments and Device Performance

Fig.1 illustrates the schematic device structure of top-gated In_2O_3 transistors with two types of substrates, 90 nm SiO_2 on p+ Si (SiO_2/Si) and 5 nm ALD grown HfO_2 at 200 °C on highly resistive Si (HfO_2/HR-Si). The HfO_2 on HR-Si is served as a thermal adhesion layer to improve the thermal interfacial conductance [10]. After the solvent cleaning of the substrate, 1.3 – 2 nm In_2O_3 was grown by ALD at 225 °C, followed by dry etching for channel isolation. Next, 40 nm Ni was deposited by e-beam evaporation as source/drain contacts. 7 nm HfO_2 top dielectric layer was grown by ALD at 120 °C [4]. Finally, 20/30 nm Ni/Au top-gate metal was deposited by e-beam evaporation, followed by O_2 annealing at 250 °C.

Electrical performance of a top-gated (TG) In_2O_3 transistor with a channel length (L_{ch}) of 200 nm and channel thickness (T_{ch}) of 1.3 nm on SiO_2/Si substrate is shown in **Fig. 2**. Drain current (I_D) of 230 μA/μm can be achieved at V_{GS} = 4 V and V_{DS} = 1 V. While higher drain current of 1 mA/μm can be obtained by reducing the L_{ch} to 40 nm [7], serious SHE will happen and make the device unstable. Therefore, it is necessary to comprehensively study device thermal properties and find a new route to further enhance device performance.

III. Steady-State Thermo-Reflectance Measurement

Fig. 3 illustrates the setup of the TR imaging system. During the TR measurement, a periodic pulsed V_{DS} signal and green light light-emitting diode (LED) are applied to the device under test (DUT). In addition, a synchronized charge-coupled device (CCD) camera is utilized to capture the surface reflectance signal from the DUT. The working mechanism of the TR imaging system is presented in **Fig. 4** [8]. The periodic pulsed V_{DS} can switch the device ON and OFF. At the ON /OFF state, the DUT heats up/cools down, and the surface reflectance signal can be captured as an active/passive image when reaching steady-state. The difference in surface reflectivity between active and passive images can be transformed into temperature rise (ΔT) by the calibrated thermal coefficient of the surface gate metal [8–11]. **Fig. 5** presents the ΔT distribution of In_2O_3 transistors with the same channel width (W_{ch}) of 2 μm but different L_{ch} from 2 μm to 600 nm. Interestingly, the ΔT near the channel center seems to be dependent on the L_{ch} of the transistors. The ΔT along channel width was extracted and normalized by power density (PD), which is defined as $(I_D\times V_{DS}) / (L_{ch}\times W_{ch})$, as shown in **Fig. 6**. It can be noticed that smaller L_{ch} devices demonstrate lower ΔT/PD, which indicates a size-dependent heat dissipation pattern in In_2O_3 transistors.

IV. Thermal Resistance Extraction

Fig. 7 presents the maximum ΔT vs. PD relation of In_2O_3 FETs with the same W_{ch} = 2 μm but different L_{ch}. Different PD is controlled by modifying V_{DS}. From the slopes of the linear regression lines of ΔT vs. PD data [12], normalized R_{TH} can be extracted and represented by the blue symbols in **Fig. 9**. An 80% reduction of R_{TH} from 11.5 to 2.1 $\times10^{-9}\cdot K\cdot m^2\cdot W^{-1}$ can be observed when L_{ch} reduces from 8 μm to 600 nm, which means a better heat dissipation in smaller L_{ch} devices. A similar trend of R_{TH} dependency on device geometry applies to devices with the same L_{ch} = 2 μm but different W_{ch} as illustrated in **Fig. 8** and **Fig. 9**. A 65% reduction of R_{TH} from 7.6 to 2.7 $\times10^{-9}\cdot K\cdot m^2\cdot W^{-1}$ with W_{ch} reducing from 8 μm to 600 nm

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further confirming the improvement of heat dissipation by scaling device dimension.

Fig. 10 illustrates the principle of L_{ch}- and W_{ch}-dependent heat dissipation in In_2O_3 devices. Joule heat generated in the channel can dissipate through five different paths: 1) vertically to the substrate, 2) laterally to the surrounding substrate, 3) laterally to the source and drain (S/D) metal, 4) vertically through gate dielectric to the gate metal, and 5) laterally through gate dielectric to the surrounding gate metal. When the L_{ch} decreases, heat dissipation from the channel to the surrounding substrate and S/D through paths 2) and 3) is enhanced, resulting in smaller R_{TH} for smaller L_{ch} devices as shown by the blue symbols in **Fig. 9**. Similarly, as the W_{ch} is scaled down, the heat dissipation via 2) and 5) is strengthened by the shorter distance between the channel and surrounding substrate and gate as illustrated by the red symbols in **Fig. 9**.

V. THERMAL CAPACITANCE EXTRACTION

In addition to R_{TH}, C_{TH} is another important parameter to learn the thermal properties of a device. In this work, a new method using steady-state and transient TR measurements as described in **Fig. 11** is proposed to extract C_{TH}. Assuming a simplified 1D thermal circuit model, our In_2O_3 transistors on the substrate can be modeled by an equivalent thermal resistor and a thermal capacitor. The value of the thermal resistor is the R_{TH} extracted from steady-state TR measurements. The normalized thermal capacitor value, C_{TH}, can be calculated by the equation [13]:

$$\tau_{TH} = R_{TH}\, C_{TH} \quad (1)$$

where τ_{TH} is the equivalent thermal time constant of the In_2O_3 FET and can be extracted from the transient TR measurement.

Fig. 12 illustrates the mechanism of the transient TR imaging system. V_{DS} pulses were set to start at 0 ns and end at 500 ns in every V_{DS} cycle [8]. Active images were first taken at t = 0 ns and a following time step of 10 – 200 ns to capture the ΔT distribution change with time as shown in **Fig. 13**. The maximum ΔT at each moment from the devices with different geometry are plotted in **Fig. 14 (a)** and **Fig. 15 (a)**. As can be seen, all transient ΔT results are similar and independent of the device geometry. To be more specific, all devices reach steady-state at around 200 ns during heat-up and cool down to $\Delta T = 0$ K at around 700 ns. **Fig. 14 (b)** and **Fig. 14 (c)** present the time constant (τ) extraction of devices with the same $W_{ch} = 2$ μm but different L_{ch} during the heat-up (τ_{heat}) and cool-down (τ_{cool}) process, respectively. The extracted τ were summarized in **Fig. 14 (d)**. Following the same process, the τ of the devices with the same $L_{ch} = 2$ μm but different W_{ch} are also extracted and summarized in **Fig. 15 (d)**. Corresponding to our observation in the transient ΔT results in **Fig. 14 (a)** and **Fig. 15 (a)**, the average thermal time constant (τ_{TH}) is independent of the transistor geometry despite some small variation. Next, using (1) and the R_{TH} from **Fig. 9**, normalized thermal capacitance (C_{TH}) can be calculated and presented in **Fig. 16**. It is found that scaling down the L_{ch} or W_{ch} of the devices can both increase the C_{TH}. Considering the physical meaning of C_{TH}, the amount of energy required to elevate the temperature of the transistor by 1 K, a larger C_{TH} value implies a more difficult heat-up process and more efficient heat dissipation. In other words, smaller devices would have better heat dissipation capability because of their larger C_{TH}, which corresponds to previous R_{TH} results in section IV. To verify the extracted C_{TH}, theoretical normalized-thermal capacitance ($C_{TH,\ theory}$) was calculated by the equation [14]:

$$C_{TH,\ theory} = M \cdot C_P / (L_{ch} \cdot W_{ch}) = A_{heat} \cdot t_{sub} \cdot \rho_{sub} \cdot C_P / (L_{ch} \cdot W_{ch}) \quad (2)$$

where M, A_{heat}, and t_{sub} (SiO_2: 90 nm) are the mass, area, and thickness of the substrate that participates in the heat dissipation, respectively. C_P is the specific heat of the substrate (SiO_2: 725 J/(kg·K) [15]). ρ_{sub} is the density of the substrate (SiO_2: 2210 kg/m^3 [15]). $C_{TH,\ theory}$ is normalized by the area ($L_{ch} \cdot W_{ch}$) of the In_2O_3 FET. If assuming $A_{heat} = L_{ch} \cdot W_{ch} = 2$ μm·2 μm, the according $C_{TH,\ theory} = 0.14$ J·K^{-1}·m^{-2} is smaller than the experimental $C_{TH} = 9.51$ J·K^{-1}·m^{-2}. Nevertheless, if considering the lateral heat dissipation through 2), 3), and 5) paths, which means the A_{heat} is larger than the device area ($L_{ch} \cdot W_{ch}$), and using $A_{heat} = 16$ μm·16 μm, the $C_{TH,\ theory} = 9.23$ J·K^{-1}·m^{-2} would be close to the experimental C_{TH}. This suggests a large portion of lateral heat dissipation as assumed in **Fig. 10**.

The R_{TH} and C_{TH} of the In_2O_3 FETs on HfO_2/HR-Si substrate are also extracted. **Fig. 17** exhibits that the device on HfO_2/HR-Si substrate has lower ΔT than SiO_2/Si substrate at similar PD because of higher thermal conductivity of Si substrate [7–10]. The R_{TH} and C_{TH} of HfO_2/HR-Si substrate shown in **Fig. 18** convey the same idea that HfO_2/HR-Si substrate has better heat dissipation capability. For example, for the device with W_{ch} of 2 μm and L_{ch} of 6 μm, **Fig. 18 (b)** demonstrates that the HfO_2/HR-Si substrate increases the C_{TH} by about 73% compared to SiO_2/Si one. It should be noted that scaling the size of the In_2O_3 transistors is also critical for heat dissipation. By reducing the L_{ch} from 6 μm to 600 nm, the C_{TH} is enhanced by 379% as plotted in **Fig. 18 (b)**.

VI. CONCLUSION

In summary, the R_{TH} and C_{TH} of ALD In_2O_3 transistors are first determined by employing the TR imaging system. Through analyzing the extracted R_{TH} and C_{TH}, it is found that the device geometry is crucial to the heat dissipation of the devices due to the lateral heat dissipation to the surrounding substrate, S/D, and gate metal, besides using a high thermal conductive substrate. The proposed extraction methods for R_{TH} and C_{TH} provide a way to quantify the thermal properties of thin film transistors, which is essential to mitigate the SHE for future monolithic 3D integration. The work is supported by AFOSR, SRC nCore IMPACT Center, and DARPA/SRC JUMP ASCENT Center.

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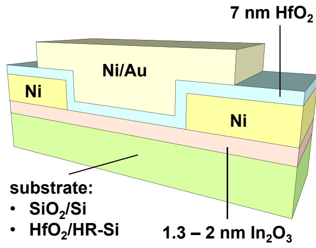


Fig. 1. Schematic device structure of top-gated (TG) In_2O_3 transistors with different substrates.

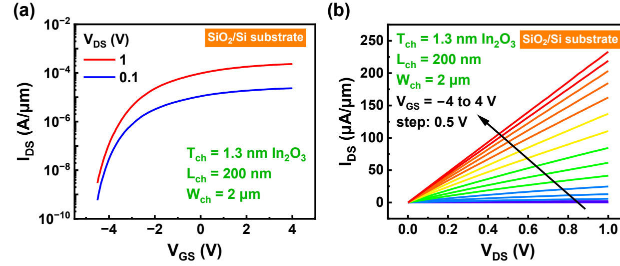


Fig. 2. (a) Transfer and (b) output characteristics of a TG In_2O_3 transistor with channel thickness (T_{ch}) of 1.3 nm, channel length (L_{ch}) of 200 nm, and channel width (W_{ch}) of 2 µm.

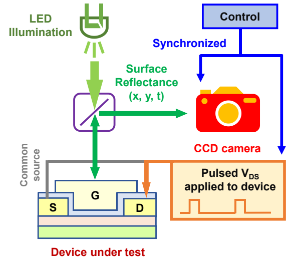


Fig. 3. Schematic of the thermo-reflectance (TR) imaging system setup.

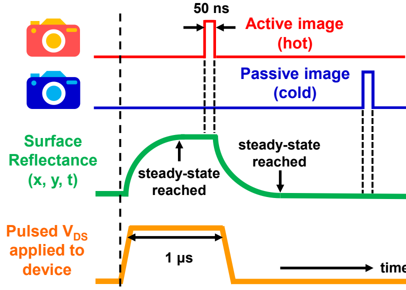


Fig. 4. Working mechanism of the steady-state TR imaging system [8].

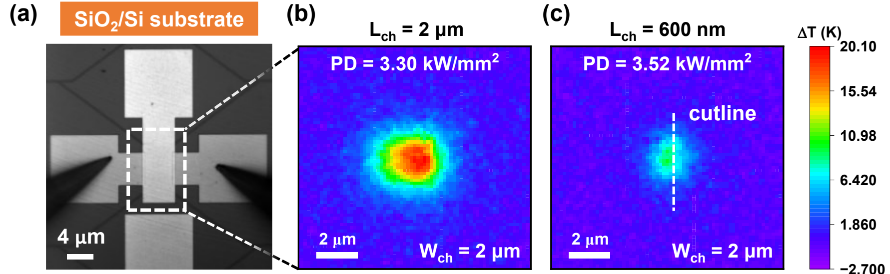


Fig. 5. (a) CCD image of the top view of an In_2O_3 transistor. TR images of devices with the same W_{ch} = 2 µm, T_{ch} = 2 nm, but different L_{ch} = (b) 2 µm and (c) 600 nm.

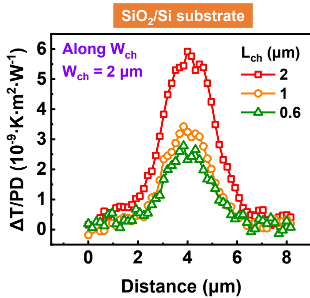


Fig. 6. Cross-sections of the normalized temperature rise (ΔT/PD) along channel width direction (cutline in Fig. 5) with various L_{ch}.

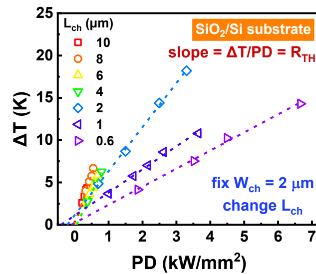


Fig. 7. Maximum ΔT of In_2O_3 devices with the same W_{ch} = 2 µm and T_{ch} = 2 nm but different L_{ch} at various PD.

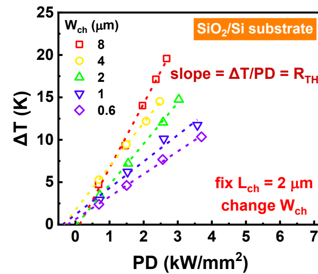


Fig. 8. Maximum ΔT of In_2O_3 devices with the same L_{ch} = 2 µm and T_{ch} = 2 nm but different W_{ch} at various PD.

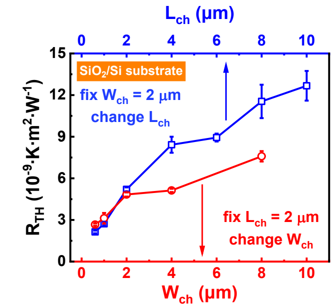


Fig. 9. Extracted normalized thermal resistance (R_{TH}). Blue symbols represent R_{TH} at different L_{ch} (extracted from Fig. 7). Red symbols represent R_{TH} at different W_{ch} (extracted from Fig. 8). It shows the heat is easier to dissipate to thick Ni S/D.

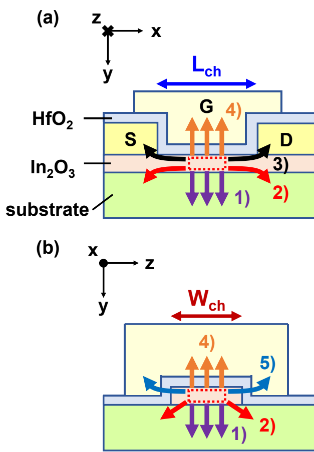


Fig. 10. Schematic cross-sections of In_2O_3 transistors showing heat dissipation path (indicated by arrows) along (a) L_{ch} and (b) W_{ch} directions.

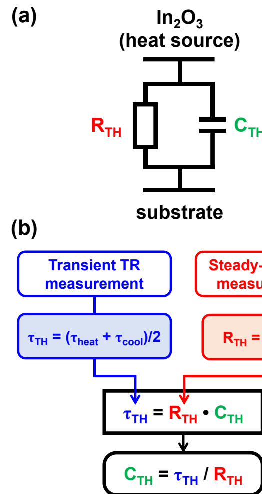


Fig. 11. (a) Simplified 1D equivalent thermal circuit model of In_2O_3 FETs. (b) Extraction method of thermal capacitance (C_{TH}).

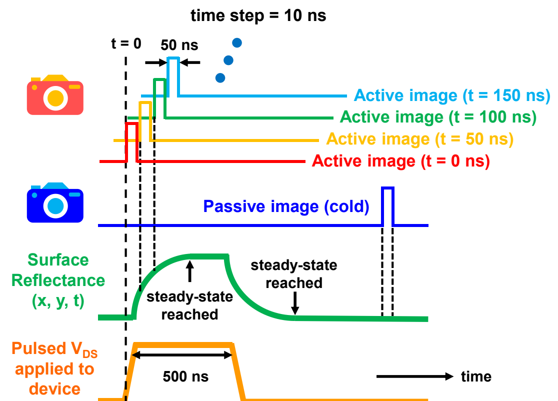
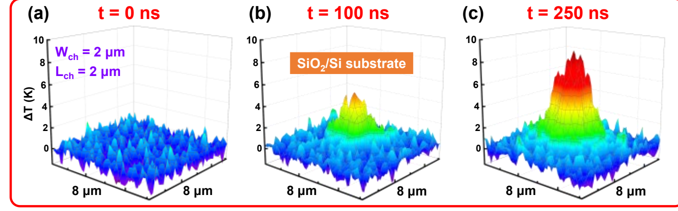


Fig. 12. Working mechanism of transient TR imaging system. V_{DS} pulses were set to start at 0 ns and end at 500 ns in every V_{DS} cycle [8].



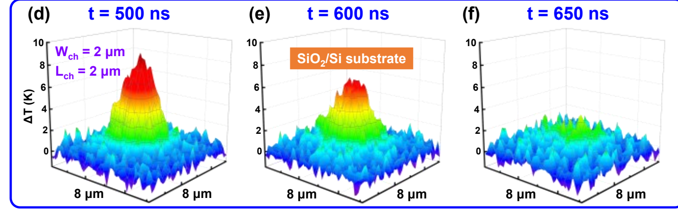


Fig. 13. Experimental transient TR image measurement of an In_2O_3 device with W_{ch} = L_{ch} = 2 μm and T_{ch} = 2 nm. (a – c) exhibit the ΔT distribution of the channel during heat-up process. (d – f) exhibit the ΔT distribution of the channel during cool-down process.

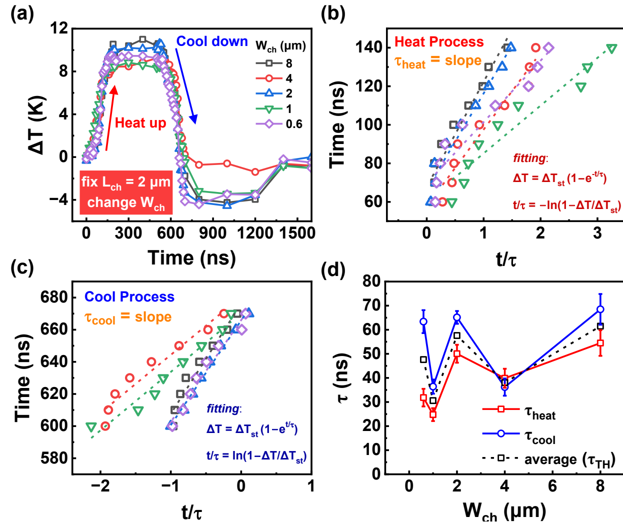


Fig. 15. (a) Transient ΔT results of In_2O_3 transistors with the same L_{ch} = 2 μm and T_{ch} = 2 nm but different W_{ch} on SiO_2/Si substrate. Time constant extraction of (b) heat-up and (c) cool-down process. (d) Extracted time constant at different W_{ch}.

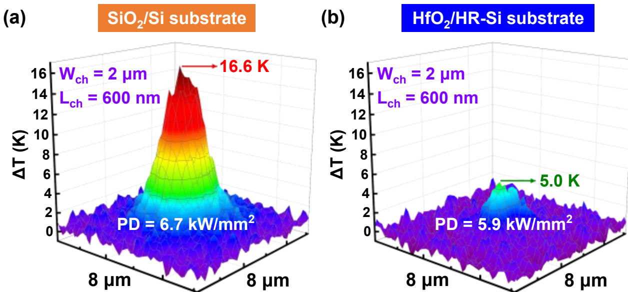


Fig. 17. Steady-state TR images of In_2O_3 devices with W_{ch} = 2 μm, L_{ch} = 600 nm, and T_{ch} = 2 nm on (a) SiO_2/Si and (b) HfO_2/HR-Si substrate. The highest ΔT in the devices was decreased from 16.6 to 5.0 K by changing the substrate material.

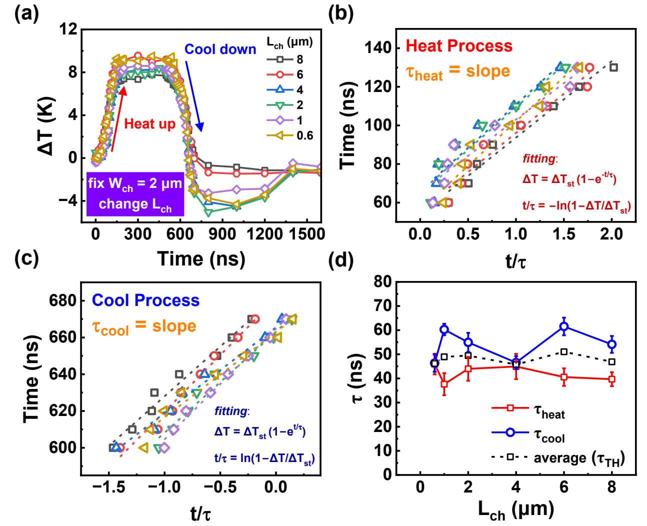


Fig. 14. (a) Transient ΔT results of In_2O_3 transistors with the same W_{ch} = 2 μm and T_{ch} = 2 nm but different L_{ch} on SiO_2/Si substrate. The ΔT from different devices were adjusted to similar level by choosing proper PD. Time constant extraction of (b) heat-up and (c) cool-down process. $ΔT_{st}$ represents the steady-state ΔT in each device. The time (t)/τ values are calculated by the fitting formulas in (b) and (c). (d) Extracted time constant at different L_{ch}.

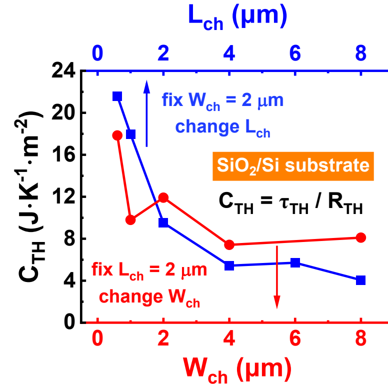


Fig. 16. Normalized thermal capacitance (C_{TH}) extracted using the thermal time constant ($τ_{TH}$) in Fig. 14 (d) and Fig. 15 (d). Blue symbols represent the C_{TH} at different L_{ch}. Red symbols represent the C_{TH} at different W_{ch}.

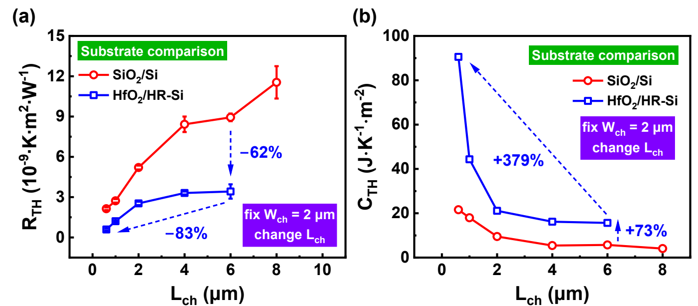


Fig. 18. Comparison of thermal parameters, (a) R_{TH} and (b) C_{TH}, of devices with the same W_{ch} = 2 μm and T_{ch} = 2 nm but different L_{ch} on SiO_2/Si and HfO_2/HR-Si substrates. Since $τ_{TH}$ is independent of device geometry, $τ_{TH}$ = 53.5 ns on HfO_2/HR-Si substrate was extracted from the In_2O_3 device with W_{ch} = L_{ch} = 2 μm and used to calculate the C_{TH} of In_2O_3 FETs on HfO_2/HR-Si substrate.